What is claimed is:

1. A nonvolatile semiconductor memory device comprising:

a memory cell array in which a plurality of memory cells are arranged in a row direction and a column direction,

wherein the memory cell array includes:

a plurality of source line diffusion layers, each of the source line diffusion layers extending along the row direction and connecting in common with the memory cells arranged in the row direction,

a plurality of bitline diffusion layers,

a plurality of element isolation regions which separate each of the bitline diffusion layers, and

a plurality of word gate common connection sections,

wherein each of the memory cells includes one of the source line diffusion layers, one of the bitline diffusion layers, a channel region between the one source line diffusion layer and the one bitline diffusion layer, a word gate and a select gate which are disposed to face the channel region, and a nonvolatile memory element formed between the word gate and the channel region,

wherein two of the word gates are formed between two of the select gates adjacent in the column direction, and one of the bitline diffusion layers is formed between the two word gates,

wherein each of the word gate common connection sections is connected in common with the two word gates above at least one of the element isolation regions, and

wherein a plurality of word gate wiring layers are formed above the word gate common connection sections, and each of the word gate wiring layers is connected with at least one word gate interconnection which is connected with one of the word gate

common connection sections.

2. The nonvolatile semiconductor memory device as defined in claim 1,

wherein an insulator is formed under the two word gates, and each of the word gate common connection sections includes a conductor which is connected in common with the two word gates formed on the insulator.

3. The nonvolatile semiconductor memory device as defined in claim 2,

wherein the insulator is formed by continuously forming the same material as a material for the nonvolatile memory element.

4. The nonvolatile semiconductor memory device as defined in claim 1,

wherein the word gate common connection sections are formed along the column direction.

5. The nonvolatile semiconductor memory device as defined in claim 1, further comprising:

a bitline connection section which is provided between one of the word gate common connection sections and one of the element isolation regions adjacent to the one word gate common connection section in the row direction, and connects one of the bitline diffusion layers with one of a plurality of bitlines.